

Nano-Net 2007 Technical Program

| Monday, September 24, 2007 | |
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| 8:00 am | Registration |
| 9:00 am - 10:00 am | Keynote 1: EI-Hang Lee - Micro/Nano-Scale Optical Circuits and Networks: A New Challenge Toward Next Generation |
| 10:00 am - 10:30 am | Break |
| 10:30 am - 12:30 pm | Session 1: Nanoscale Architecture and Coding |
| 10:30 am | Fault Tolerant Nano-Memory with Fault Secure Encoder and Decoder <i>Helia Naeimi , Andre DeHon</i> |
| 11:00 am | Analysis of Forward Error Correction Methods for Nanoscale Networks-On-Chip <i>Teijo Lehtonen , Pasi Liljeberg , Juha Plosila</i> |
| 11:30 am | A 90nm CMOS Cryptographic Core with Improved Fault-Tolerance in Presence of Massive Defect Density <i>Alexandre Schmid</i> |
| 12:00 pm | Integrated Waveguides for Ultra-High Speed Interconnects (invited) <i>D. Urbano, E. Arneri, G. Cappuccino, G. Amendola</i> |
| 12:30 pm - 2:00 pm | Lunch |
| 2:00 pm – 3:30 pm | Session 2: Optical Networks and NEMS |
| 2:00 pm | Semi-Analytic Model for Dispersion Relation of Nanowire Lasers <i>Mohammad Karami</i> |
| 2:30 pm | Spectral Sensing with Coupled Nanoscale Oscillators <i>Nikolai Nefedov</i> |
| 3:00 pm | Suspended-gate MOSFET for low standby power switch and memory applications (invited) <i>D. Tsamados, A.M. Ionescu</i> |
| 3:30 pm – 4:00 pm | Break |
| 4:00 pm – 5:30 pm | Session 3: Networks-on-Chip – Implementation Issues |
| 4:00 pm | A methodology and a case-study for Network-on-Chip based MP-SoC architectures <i>Sergio Tota , Mario Casu , Maurizio Zamboni , Paolo Motto , Massimo Roch</i> |
| 4:30 pm | Relieving physical issues in new NoC-based SoC <i>Daniele Mangano</i> |
| 5:00 pm | Dual-Channel Binary-Countdown Medium Access Control in Wireless Network-on-Chip <i>Danella Zhao</i> |
| 6:00 pm – 8:00 pm | Reception (TBD) |

Tuesday, September 25, 2007

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| 8:30 am | Registration |
| 9:00 am - 10:00 am | Keynote 2: TBD (ST) |
| 10:00 am - 10:30 am | Break |
| 10:30 am - 12:30 pm | Session 4: Networks-on-Chip – Topology Issues |
| 10:30 am | A Topology Design Customization Approach for STNoC <i>Gianluca Palermo , Riccardo Locatelli , Marcello Coppola , Cristina Silvano</i> |
| 11:00 am | Algorithm for the Choice of Topology in Reconfigurable On-Chip Networks with Real-Time Support <i>Kristina Kunert , Mattias Weckstén , Magnus Jonsson</i> |
| 11:30 am | Topology-Unaware Routing in Irregular Self-Assembled Networks-on-Chip: An Explorative Case Study <i>Christof Teuscher</i> |
| 12:00 pm | Supporting vertical links for 3D networks on chip: toward an automated design and analysis flow <i>Igor Loi</i> |
| 12:30 pm - 2:00 pm | Lunch |
| 2:00 pm – 3:30 pm | Session 5: Optoelectronic Nanodevices |
| 2:00 pm | Au, Ag and Cu-Silicon RCE photodetectors based on the internal photoemission effect at 1.55 micron <i>Maurizio Casalino, L. Sirleto, L. Moretti, Francesco Della Corte, I. Rendina</i> |
| 2:30 pm | Raman Approach in Silicon Nanostructure at 1.5 micron <i>L. Sirleto, Maria Ferrara, B. Jalali, I. Rendina</i> |
| 3:00 pm | Design, Fabrication and Characterization of an a-Si:H / SiCN waveguide multistack for electro-optical modulation <i>Sandro Rao, Maria Nigro, Francesco Suriano, Francesco Della Corte, Caterina Summonte, Alberto Scandurra</i> |
| 3:30 pm – 4:00 pm | Break |
| 4:00 pm – 5:30 pm | Session 6: Molecular and Atomistic Nanostructures |
| 4:00 pm | Development of Molecular based Communication Protocols for Nanomachines <i>Frank Walsh</i> |
| 4:30 pm | Thermodynamic Simulations of DNA Tile Self-Assembly <i>Kenichi Fujibayashi, Satoshi Murata</i> |
| 5:00 pm | Networking Behavior in Thin Film and Nanostructure Growth Dynamics <i>Murat Yuksel , Tansel Karabacak , Hasan Guclu</i> |
| 6:00 pm – 8:00 pm | Social Event (TBD) |

Wednesday, September 26, 2007

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| 8:30 am | Registration |
| 9:00 am - 10:00 am | Keynote 3: Eby Friedman - On-Chip Optical Interconnect for Reduced Delay Uncertainty |
| 10:00 am - 10:30 am | Break |
| 10:30 am - 12:00 pm | Session 7: Nanoscale Interconnect |
| 10:30 pm | Asynchronous links (invited) <i>Alex Yakovlev</i> |
| 11:00 am | Scaling and Evaluation of Carbon Nanotube Interconnects for VLSI Applications <i>Fred Chen , Ajay Joshi , Vladimir Stojanovic , Anantha Chandrakasan</i> |
| 11:30 am | Generating Reduced Order Models using Subspace Iteration for Linear RLC Circuits in Nanometer Designs <i>Ravindra Jayanthi, Srinivas Mandalika</i> |
| 12:00 pm - 1:00 pm | Panel: Future of NanoNets Conference |
| 1:00 pm | Conference closes |