

## **Nano-Net 2006 - Technical Program**

### **Day 1 – Thursday, September 14<sup>th</sup>**

**8:00 AM**      **Registration**

**9:00 AM**      **Welcome & Announcements**

9:15 AM      Keynote Speaker: Philip Kuekes, HP-Labs

**10:15 AM**      ***Coffee break***

10:45 AM      Session 1: Networks-on-Chip, Part I

Session Chair: Luca Benini

1. Novel Design of Three-Dimensional Crossbar for Future Network on Chip based on Post-Silicon Devices  
*Kumiko Nomura, Keiko Abe, Shinobu Fujita, Toshiba*  
*André M. DeHon, California Institute of Technology*
2. A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects  
*Dongkook Park, Chrysostomos Nicopoulos, Jongman Kim,*  
*N. Vijaykrishnan, Chita R. Das, Pennsylvania State University*
3. A Low Cost Network-on-Chip with Guaranteed Service Well Suited to the GALS Approach  
*Ivan Miro Panades, STMicroelectronics,*  
*Alain Greiner, Abbas Sheibanyrad, Universite Pierre et Marie Curie*
4. A Theoretical Framework for On-chip Stochastic Communication Analysis  
*Radu Marculescu, Carnegie Mellon Institute*
5. Area and Power Modeling Methodologies for Networks-on-Chip  
*Paolo Meloni, Salvatore Carta, Roberto Argiolas,*  
*Luigi Raffo, University of Cagliari,*  
*Federico Angiolini, University of Bologna*

**12:50 PM**      ***Lunch break***

2:15 PM      Session 2: Architectures and Systems for Nano-Networks,  
Session Chair: Alvin Lebeck

1. *(Invited)* The State of ZettaRAM  
*Eric Rotenberg*, North Carolina State University  
*Ravi K. Venkatesan*, Intel
2. 3D Nanowire-Based Programmable Logic  
*Benjamin Gojman*, *Raphael Rubin*, *Concetta Pilotto*,  
*André M. DeHon*, California Institute of Technology,  
*Tetsufumi Tanamoto*, Toshiba
3. Connecting and Configuring Defective Nano-Scale Networks for DNA Self-Assembly  
*Luke Demoracski*, *Fabrizio Lombardi*, Northeastern University
4. Design and Simulation of Logic Circuits with Hybrid Architectures of Single Electron Transistors and Conventional Devices  
*A. Venkataratnam*, *A. K. Goel*, Michigan Technological University

**3:55 PM**      *Coffee break*

4:25 PM      Session 3: Innovative System Interconnects, Part I  
Session Chair: Adrian Ionescu

5. *(Invited)* Can Carbon Nanotubes Extend the Lifetime of On-Chip Electrical Interconnections?  
*Kaustav Banerjee*, *Sungjun Im* and *Navin Srivastava*, University of California – Santa Barbara
6. Electron beam-induced light emission and transport in GaN nanowires  
*Joseph Tringe*, *Warren Moberly Chan*,  
*Charles Stevens*, Lawrence Livermore National Laboratory,  
*Albert Davydov*, *Abhishek Motayed*, National Institute of Standards and Technology
7. Optimizing Dielectric Strip Plasmonic Waveguides for Subwavelength On-Chip Optical Communication  
*Amir Hosseini*, *Arthur Nieuwoudt*, *Yehia Massoud*, Rice University
8. Future Trends on Nanoantennas Synthesis  
*Davide Franceschini*, *Massimo Donelli*, *Renzo Azaro*,  
*Andrea Massa*, University of Trento

**6:05 PM**      **Day 1 Conclusion**

## Day 2 – Friday, September 15<sup>th</sup>

8:00 AM Registration

9:00 AM Welcome & Announcements

9:15 AM Keynote Speaker: Giovanni De Micheli, EPFL – “*Design Technologies for Nanosystems On Chip*”

10:15 AM *Coffee break*

10:45 AM Session 4: Innovative System Interconnects, Part II

Session Chair: Adrian Ionescu

9. Multipolar Photonic Interactions for Interconnections and Logical Operations in Nanostructure Networks

*Hideaki Matsueda, Kochi University*

10. (Invited) Hybrid Nanostructures: Organic Interconnections and Device Applications

*Sandro Carrara, Bruno Samorì, University of Bologna,  
Sigrid Bernstorff, Marina Di Pasquale, Alberto Ansaldo, Maria Teresa Parodi, Davide Ricci, Ermanno Di Zitti, University of Genoa*

11. Optical Interconnects for Network on Chip

*Alberto Scandurra, Maurizio Lenzi, Ranieri Guerra, STMicroelectronics,  
Francesco G. Della Corte,  
M. Arcangela Nigro, DIMET - Mediterranea University*

12. Controlled nanowire fabrication by PEDAL process

*Sachin R. Sonkusale, Paul Franzon, North Carolina State University*

13. On-Chip Interconnects and Repeaters Based on NiSi Nanowires

*Adam Maina Ari, Woon Ket Wong,  
Wei Wang, Indiana University – Purdue University Indianapolis*

12:50 PM *Lunch break*

2:15 PM Session 5: Modeling, and Simulation of Nano-Networks,

Session Chair: Vijaykrishnan Narayanan

14. Self-Assembled Networks: Control vs. Complexity

*Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, Duke University*

15. (Invited) Predictive Technology Model for Nano-CMOS Design Exploration

*Yu Cao, Wei Zhao, Arizona State University*

16. *(Invited)* Modeling and Evaluating Carbon Nanotube Bundles for Future VLSI Interconnect Applications

*Yehia Massoud, Arthur Nieuwoudt, Rice University*

**3:30 PM**      *Coffee break*

3:50 PM      Session 6: Networks-on-Chip, Part II

Session Chair: Luca Benini

17. Routing Aware Switch Hardware Customization for Networks on Chips

*Paolo Meloni, Massimo Camplani, Luigi Raffo,  
Salvatore Carta, University of Cagliari,  
Srinivasan Murali, Stanford University,  
Giovanni De Micheli, EPFL*

18. Skew Insensitive Physical Links for Network on Chip

*Daniele Mangano, Riccardo Locatelli, Alberto Scandurra, Carlo Pistrutto,  
Marcello Coppola, STMicroelectronics,  
Luca Fanucci, Francesco Vitullo, Dario Zandri, University of Pisa*

19. *(Invited)* 3D on-chip networking technology based on post-Silicon devices for Future Network on Chip

*Shinobu Fujita, Kumiko Nomura, Keiko Abe, Toshiba,  
Thomas H. Lee, Stanford University*

20. Reliability Analysis for On-chip Networks

*Yehia Massoud, Xiang Wu, Mosin Mondal, Adnan Aziz, Rice University*

**5:30 PM**      **Day 2 Conclusion**

**6-8 PM**      **Social Event (Olympic Museum, Lausanne)**

## Day 3 – Saturday, September 16<sup>th</sup>

8:00 AM Registration

9:00 AM Welcome & Announcements

9:15 AM Session 7: Information Theory Aspects of Nano-Networks,  
Session Chair: G.M. Maggio

21. *(Invited)* Graph Spectra of Carbon Nanotube Networks  
*Stephen F. Bush*, GE Research  
*Sanjay Goel*, University at Albany
22. On Information Transmission Among Nanomachines  
*Giusi Alfano*, Università di Napoli “Frederico II”,  
*Daniele Miorandi*, Create-Net
23. *(Invited)* Nanoscale Data Storage Devices, their Capacity and Data Encoding Schemes  
*Paul P. Sotiriadis*, Johns Hopkins University

10:30 AM Coffee break

11:00 AM Panel Discussion: Design Challenges for Nanotechnology-based Nanoelectronics - Can we build systems with nanodevices?

*Tim Ashley*, QinetiQ  
*Ali Javey*, University of California – Berkeley  
*Ali Keshavarzi*, Intel  
*Philip Keukes*, HP-Labs  
*Azad Naeemi*, Georgia Institute of Technology  
*Carlo Pistrutto*, STMicroelectronics  
*Kazuo Yano*, Hitachi

12:45 PM Day 3 Conclusion