

Nano-Net 2006

1st International Conference on Nano-Networks



Lausanne, Switzerland,
September 14-16, 2006
www.nanonets.org



*Sponsors: CREATE-NET, ICST, EU (IST-FET), ENIAC, IEEE CAS & CEDA
In Cooperation with: IEEE-TCCA, Industry Sponsor: STMicroelectronics*



Welcome to Nano-Net 2006!

Message from the Conference General Co-Chairs:

Dear Participants,

It is our great pleasure to welcome all of you to **Nano-Net 2006**, the First International Conference on Nano-Networks!

The event is organized by CREATE-NET, in technical cooperation with the IEEE-TCCA, and sponsored by the IEEE CAS & CEDA, ICST, the European Union (IST-FET) and ENIAC, while the main industry sponsor is STMicroelectronics. The Conference is being held at the prestigious Swiss Federal Institute of Technology, Lausanne (EPFL) on the beautiful Geneva Lake area, in Switzerland.

The Conference scope is at the cutting-edge, positioned to cover the intersection between emerging nanoscale devices and interconnect systems. Discovery at this interface is sustained by an interest in building systems from unprecedented numbers of nanoscale devices into complex and highly integrated systems. The challenges that face this pursuit are varied and substantial, yet we can make significant progress today by beginning to understand the changing relationships between devices, interconnect, and systems driven by the fundamental opportunities presented by nanotechnology. Likewise, new paradigms in information theory are necessary to analyze and design tomorrow's nanoscale communication networks.

The First Edition of the Nano-Net Conference is organized as a single-track high-quality event, featuring a premium Technical Program, with presentations delivered by world-class scientists and top industry experts. We have two exciting keynote speakers to kick-off the event: Philip Keukes of HP-Labs and Prof. Giovanni De Micheli of EPFL will share with us their visions about nanoscale interconnect and systems and the opportunities available to us as a field. Our Technical Program this year covers a wide spectrum of topics from nanoscale networks-on-chip and carbon nanotube interconnect modeling, to nanoscale wireless transmission and 3D nanowire integration. An outstanding Panel, organized by Intel, addressing design challenges for nanoelectronics will close the event. We are confident that you will find many interesting conversions during the program!

Finally, we thank you all for your participation as well as the many Committee Members' hard work that has contributed to the success of the Nano-Net 2006 Conference. We invite you to take part in and to enjoy the conference.

With Best Regards,



Chris Dwyer



Gian Mario Maggio



Nano-Net 2006 - Technical Program

Day 1 – Thursday, September 14th

8:00 AM Registration

9:00 AM **Welcome & Announcements**

9:15 AM Keynote Speaker: Philip Kuekes, HP-Labs

10:15 AM **Coffee break**

10:45 AM Session 1: Networks-on-Chip, Part I

Session Chair: Luca Benini

1. Novel Design of Three-Dimensional Crossbar for Future Network on Chip based on Post-Silicon Devices
Kumiko Nomura, Keiko Abe, Shinobu Fujita, Toshiba
André M. DeHon, California Institute of Technology
2. A Distributed Multi-Point Network Interface for Low-Latency, Deadlock-Free On-Chip Interconnects
Dongkook Park, Chrysostomos Nicopoulos, Jongman Kim,
N. Vijaykrishnan, Chita R. Das, Pennsylvania State University
3. A Low Cost Network-on-Chip with Guaranteed Service Well Suited to the GALS Approach
Ivan Miro Panades, STMicroelectronics,
Alain Greiner, Abbas Sheibanyrad, Universite Pierre et Marie Curie
4. A Theoretical Framework for On-chip Stochastic Communication Analysis
Radu Marculescu, Carnegie Mellon University
Paul Bogdan, Carnegie Mellon University
5. Area and Power Modeling Methodologies for Networks-on-Chip
Paolo Meloni, Salvatore Carta, Roberto Argiolas,
Luigi Raffo, University of Cagliari,
Federico Angiolini, University of Bologna

12:50 PM **Lunch break**



2:15 PM Session 2: Architectures and Systems for Nano-Networks,
Session Chair: Alvin Lebeck

1. *(Invited)* The State of ZettaRAM
Eric Rotenberg, North Carolina State University
Ravi K. Venkatesan, Intel
2. 3D Nanowire-Based Programmable Logic
Benjamin Gojman, Raphael Rubin, Concetta Pilotto,
André M. DeHon, California Institute of Technology,
Tetsufumi Tanamoto, Toshiba
3. Connecting and Configuring Defective Nano-Scale Networks for DNA Self-Assembly
Luke Demoracski, Fabrizio Lombardi, Northeastern University
4. Design and Simulation of Logic Circuits with Hybrid Architectures of Single Electron Transistors and Conventional Devices
A. Venkataratnam, A. K. Goel, Michigan Technological University

3:55 PM *Coffee break*

4:25 PM Session 3: Innovative System Interconnects, Part I
Session Chair: Adrian Ionescu

5. *(Invited)* Can Carbon Nanotubes Extend the Lifetime of On-Chip Electrical Interconnections?
Kaustav Banerjee, Sungjun Im and Navin Srivastava, University of California – Santa Barbara
6. Electron beam-induced light emission and transport in GaN nanowires
Joseph Tringe, Warren Moberly Chan,
Charles Stevens, Lawrence Livermore National Laboratory,
Albert Davydov, Abhishek Motayed, National Institute of Standards and Technology
7. Optimizing Dielectric Strip Plasmonic Waveguides for Subwavelength On-Chip Optical Communication
Amir Hosseini, Arthur Nieuwoudt, Yehia Massoud, Rice University
8. Future Trends on Nanoantennas Synthesis
Davide Franceschini, Massimo Donelli, Renzo Azaro,
Andrea Massa, University of Trento

6:05 PM **Day 1 Conclusion**



Day 2 – Friday, September 15th

8:00 AM Registration

9:00 AM Welcome & Announcements

9:15 AM Keynote Speaker: Giovanni De Micheli, EPFL – “*Design Technologies for Nanosystems On Chip*”

10:15 AM Coffee break

10:45 AM Session 4: Innovative System Interconnects, Part II

Session Chair: Adrian Ionescu

9. Multipolar Photonic Interactions for Interconnections and Logical Operations in Nanostructure Networks
Hideaki Matsueda, Kochi University
10. (Invited) Hybrid Nanostructures: Organic Interconnections and Device Applications
Sandro Carrara, Bruno Samorì, University of Bologna, Sigrid Bernstorff, Marina Di Pasquale, Alberto Ansaldo, Maria Teresa Parodi, Davide Ricci, Ermanno Di Zitti, University of Genoa
11. Optical Interconnects for Network on Chip
Alberto Scandurra, Maurizio Lenzi, Ranieri Guerra, STMicroelectronics, Francesco G. Della Corte, M. Arcangela Nigro, DIMET - Mediterranea University
12. Controlled nanowire fabrication by PEDAL process
Sachin R. Sonkusale, Paul Franzon, North Carolina State University
13. On-Chip Interconnects and Repeaters Based on NiSi Nanowires
Adam Maina Ari, Woon Ket Wong, Wei Wang, Indiana University – Purdue University Indianapolis

12:50 PM Lunch break

2:15 PM Session 5: Modeling, and Simulation of Nano-Networks,

Session Chair: Vijaykrishnan Narayanan

14. Self-Assembled Networks: Control vs. Complexity
Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, Duke University
15. (Invited) Predictive Technology Model for Nano-CMOS Design Exploration
Yu Cao, Wei Zhao, Arizona State University
16. (Invited) Modeling and Evaluating Carbon Nanotube Bundles for Future VLSI Interconnect Applications
Yehia Massoud, Arthur Nieuwoudt, Rice University



3:30 PM *Coffee break*

3:50 PM Session 6: Networks-on-Chip, Part II

Session Chair: Luca Benini

17. Routing Aware Switch Hardware Customization for Networks on Chips
Paolo Meloni, Massimo Camplani, Luigi Raffo, Salvatore Carta, University of Cagliari, Srinivasan Murali, Stanford University, Giovanni De Micheli, EPFL
18. Skew Insensitive Physical Links for Network on Chip
Daniele Mangano, Riccardo Locatelli, Alberto Scandurra, Carlo Pistrutto, Marcello Coppola, STMicroelectronics, Luca Fanucci, Francesco Vitullo, Dario Zandri, University of Pisa
19. *(Invited)* 3D on-chip networking technology based on post-Silicon devices for Future Network on Chip
Shinobu Fujita, Kumiko Nomura, Keiko Abe, Toshiba, Thomas H. Lee, Stanford University
20. Reliability Analysis for On-chip Networks
Yehia Massoud, Xiang Wu, Mosin Mondal, Adnan Aziz, Rice University

5:30 PM **Day 2 Conclusion**

6-8 PM **Social Event (Olympic Museum, Lausanne)**



Day 3 – Saturday, September 16th

8:00 AM Registration

9:00 AM Welcome & Announcements

9:15 AM Session 7: Information Theory Aspects of Nano-Networks,
Session Chair: G.M. Maggio

21. (Invited) Graph Spectra of Carbon Nanotube Networks
Stephen F. Bush, GE Research
Sanjay Goel, University at Albany
22. On Information Transmission Among Nanomachines
Giusi Alfano, Università di Napoli “Frederico II”,
Daniele Miorandi, CREATE-NET
23. (Invited) Nanoscale Data Storage Devices, their Capacity and Data Encoding Schemes
Paul P. Sotiriadis, Johns Hopkins University

10:30 AM Coffee break

11:00 AM Panel Discussion: Design Challenges for Nanotechnology-based
Nanoelectronics - Can we build systems with nanodevices?

Tim Ashley, QinetiQ
Ali Javey, University of California – Berkeley
Ali Keshavarzi, Intel
Philip Keukes, HP-Labs
Azad Naeemi, Georgia Institute of Technology
Carlo Pistrutto, STMicroelectronics
Kazuo Yano, Hitachi

12:45 PM Day 3 Conclusion



Nano-Net 2006 Local Arrangements Information

Conference Locations

All Sessions of Nano-Net 2006 will be held in EPFL, auditorium CE1. Coffee breaks are served in the CE corridor, facing the registration desk. Please wear your conference badge during all sessions and coffee/lunch breaks.

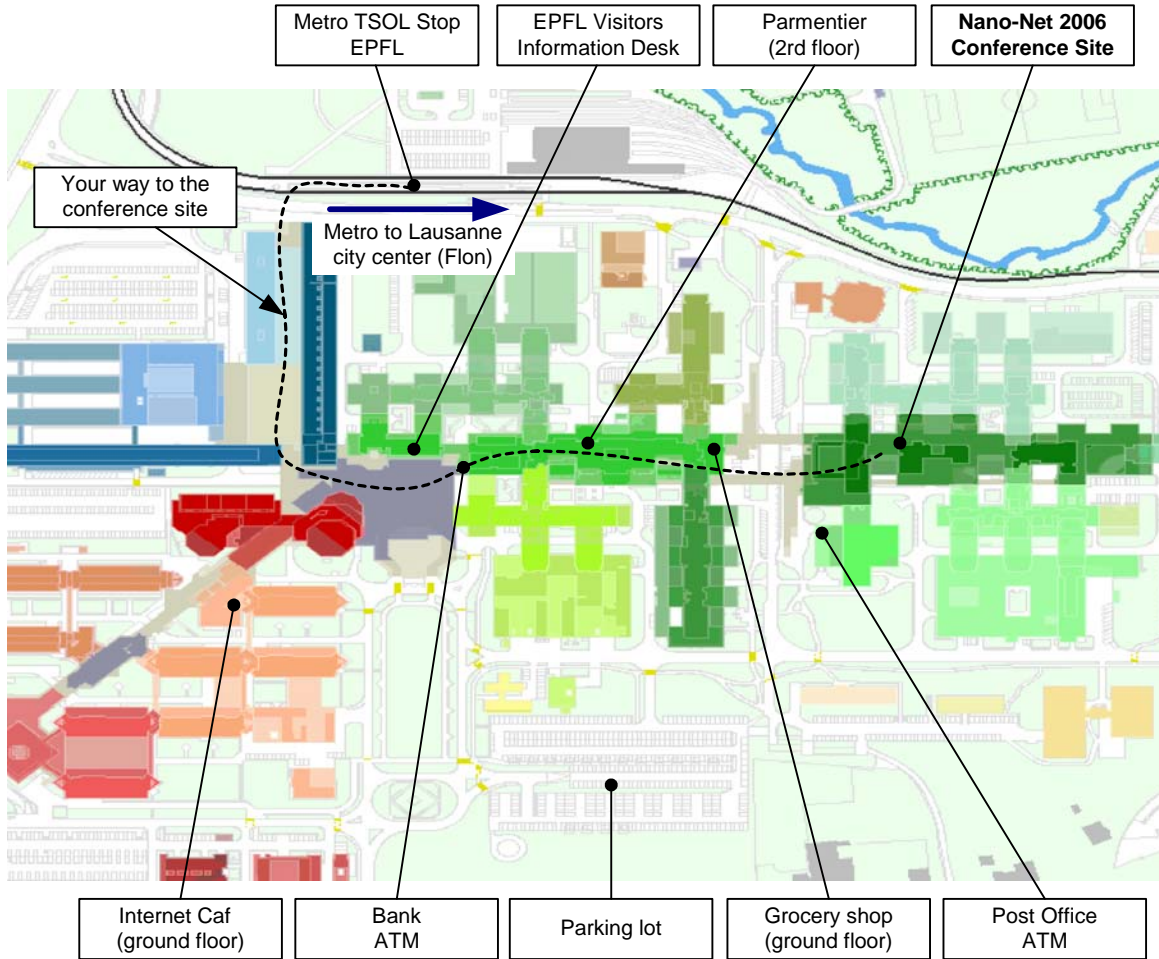
Lunch is taken in the campus restaurant Parmentier. Attendees can have lunch any time between 12 PM and 2 PM.

Parmentier is a self-service restaurant. Vegetarian meal is served upon request. A Nano-Net 2006 lunch voucher must be handed over to the cashier, covering a full course meal plus one non-alcoholic beverage.



Locations at EPFL

Several services are available on-campus, as reported on the map.




Attendees who have their car parked in the parking lot must ask for a parking card at the conference registration desk (CHF5.0/day).



Access to internet

WiFi access is provided over the EPFL campus. The computer must accept its IP from the server (DHCP). The access page is hooked up upon starting a browser (<http://enclair.epfl.ch>).

	<p>Free access is granted to Nano-Net 2006 attendees.</p> <p>The following account information must be entered.</p> <table border="1" data-bbox="798 683 1396 840"> <tr> <td>Username</td> </tr> <tr> <td>x-nano06</td> </tr> <tr> <td>Password</td> </tr> <tr> <td>Please ask the registration desk</td> </tr> </table>	Username	x-nano06	Password	Please ask the registration desk
Username					
x-nano06					
Password					
Please ask the registration desk					

Alternatively, an **Internet Café** with desktop computers has been prepared in the EL building. The computers are in the entrance hall of the building, ground floor.

Username
LEG_summer
Password
Please ask the registration desk
Domain
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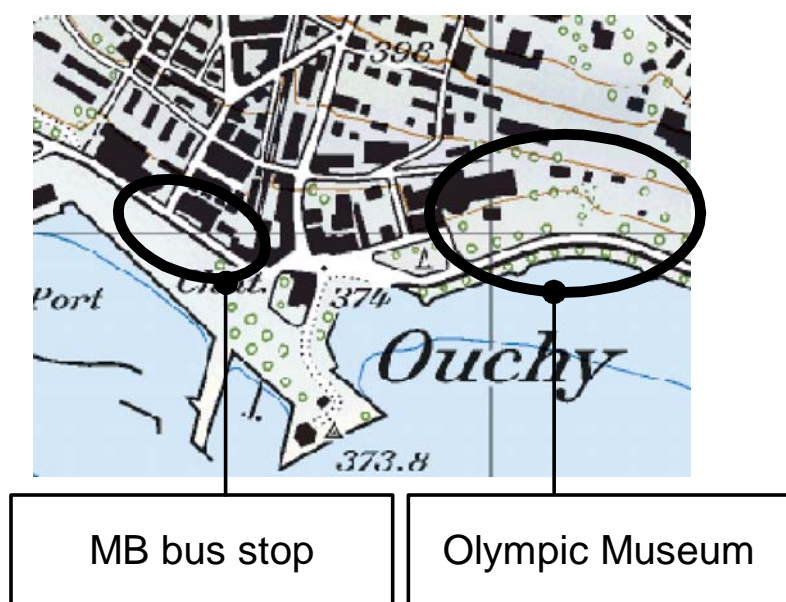
Social Event

The Nano-Net 2006 Social Event will take place at the Olympic Museum located in Lausanne-Ouchy. It will comprise a Museum visit, followed by an aperitif with some refreshments and snacks.

A bus will pick-up Nano-Net attendees on Friday at 5:30 PM (following the last session) from the bus stop located in front of the EPFL post office, to the Olympic Museum where the Social Event will start at 6 PM, and end around 8 PM.

Entrance tickets will be delivered at the entrance of the Olympic Museum. Please wear your conference badge.

Bus MB can be taken to return to downtown after the event. This bus stops in several locations, including Main Train Station, and Flon (metro connection). **A ticket must be purchased.**



Emergency Numbers

On EPFL campus, use any EPFL phone
115

In Lausanne	
Police (emergencies)	117
Fire service alarm	118
Ambulances (emergencies)	144

